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ZFx86 And The Cypress Clock Chip

ZF created this document to help you understand the ZFx86 interface to the Cypress CY2292F clock chip. This document does not describe all the features of CY2292F; it explains how to use the clock chip with any ZFx86 specific requirements, and discusses critical design issues.

Why the Cypress Clock Chip?

ZF chose the CY2292F chip, a three-PLL General Purpose EPROM Programmable Clock Generator, because it produces all the necessary clocks required by the ZFx86. This clock chip allows you to slow the CPU speed and PCI clocks, and to “on the fly” lower an application’s power consumption (not discussed in this document). Additionally, you may use one of the CY2292F’s programmed frequencies for an external device (for example, the Network interface, or the CRT controller).

Additional Software Tools Required

To program the CY2292F clock chip, you need the Cypress Programmer Clocks Programming Kit **CY6730 FTG**. This kit includes the proper adapter and programming software, CyClock version 3.65.

ZF Recommendations

When using the CY2292F chip, standard power filtering, that is using a 0.1uF ceramic capacitor in either side of the clock chip, is sufficient filtering for most designs. However when using one or more clock outputs for peripheral devices (for example, the Network or CRT controller) you must give more consideration to power filtering, for example, a Linear Regulator might be required on the clock chip.

ZF’s design experience indicates that a buffered reference clock output (XBUF) is stable when you use standard power filtering. However, to achieve similar results with any synthesized clock outputs, you must take special care when filtering CY2292F power. Because the synthesized clock outputs definitely require more components, we recommend you choose the correct reference clock and use its buffered output when a critical low jitter clock output is required, for example, a 10/100 network chip, or CRT/Flat panel controllers. When you require a 25 MHz clock for the 10/100 Network controller, we recommend you use a 25 MHz reference crystal (see our second sample found on page 4).

ZFx86 Clocking Requirements

With some limitations the ZFx86 will operate using a single 48MHz clock. However for the chip to be fully operational, it needs the following clock signals:

- USB Clock 48.000 MHz
- Timer Clock 14.318 MHz
- System Clock up to 64 MHz
- PCI Clock up to 33 MHz
- Real Time Clock 32.768 KHz

The CY2292F provides the first four clock signals. For the Real Time Clock signal, use an external crystal together with external Real Time Clock battery.

Two Sample Configurations

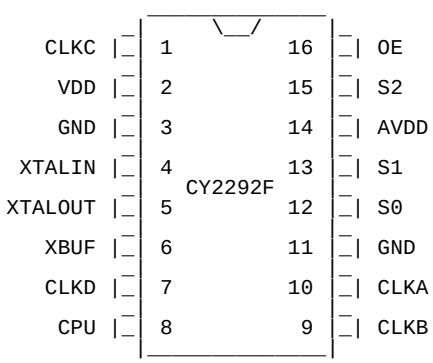
First Sample Using The 14.31818 MHz Clock Output

The first sample configuration uses a 14.31818 MHz reference crystal together with the CY2292F chip. Connect the clock signals in following order:

1. Use the XBUF = 14.31818 MHz output for the Timer Clock (in this case no programming is needed, as this is the buffered reference crystal output).
2. Connect the CPUCLK = 64 MHz output to the System Clock.
3. Connect the CLKA = 48 MHz output to the USB clock.
4. Use the CLKB, CLKC and CLKD = 64/2=32 MHz output as PCI clocks.

As a result, Figure 1 illustrates the Cypress Clock software printout using the above configuration.

```
  _____  _____ ___ ___ ___ ___
 / __\ \ / / _ \ _ \ __/ __/ __|
| (__ \ ^ /|  _/   / _|\__ \__ \
 \___| |_| |_| |_|_\___|___/___/ TIMING TECHNOLOGY
================================================
Modification Date: Jun/15/2001
Comments: Sample Configuration 1
Customer: ZF Micro Devices, Inc.
FAE: Kaido Kevvai
P/N: CY2292FSC
```




```
Reference Input: 14.31818 MHz
Operating Voltage: 3.3V
CPLL: --
SPLL: Desired = Off
UPLL: Desired = 48 MHz
```

CPLL FREQUENCIES

S2:S0	Desired	Actual	PPM	Option
000	64.00000	63.99350	-102	--
001	Off	--	--	--
010	Off	--	--	--
011	Off	--	--	--
100	Off	--	--	--
101	Off	--	--	--
110	Off	--	--	--
111	Off	--	--	--

OUTPUT CLOCKS

	Desired	Actual	PPM	Option
CPU	CPLL	CPLL	--	--
CLKA	UPLL (48.00000)	47.99844	-32	--
CLKB	CPLL/2	CPLL/2	--	--
CLKC	CPLL/2	CPLL/2	--	--
CLKD	CPLL/2	CPLL/2	--	--
XBUF	Ref (14.31818)	14.31818	0	--

ACTUAL OUTPUT FREQUENCIES

S2:S0	CPU	CLKA	CLKB	CLKC	CLKD	XBUF
000	63.99350	47.99844	31.99675	31.99675	31.99675	14.31818
001	Off	47.99844	Off	Off	Off	14.31818
010	Off	47.99844	Off	Off	Off	14.31818
011	Off	47.99844	Off	Off	Off	14.31818
100	Off	47.99844	Off	Off	Off	14.31818
101	Off	47.99844	Off	Off	Off	14.31818
110	Off	47.99844	Off	Off	Off	14.31818
111	Off	47.99844	Off	Off	Off	14.31818

```
Entry File: Sample1.ent
CHECKSUM: 230
(Generated by CyClocks(tm) 3.65 - Build #: 3.65.003)
```

Figure 1. Cypress Chip 14.31818 MHz Clock Output

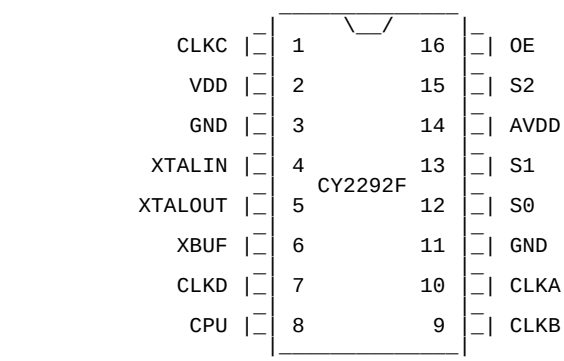
Second Sample Using The 25MHz Clock Output

To produce a low jitter, stable 25 MHz Clock for a Network chip, it is wise to use 25 MHz crystal as a source instead of the 14.31818 MHz as in the first sample. In this case, we used the buffered crystal output XBUF as a clock for Network chip instead of using a synthesized clock signal.

1. Use the XBUF = 25 MHz output for the Network Chip clock. (in this case no programming is needed, as this is the buffered reference crystal output).
2. Connect the CPUCLK = 64 MHz output to the System Clock.
3. Connect the CLKA = 48 MHz output to USB clock.
4. Connect the CLKB = 14.31818 MHz output to the Timer Clock.
5. Use the CLKC and CLKD = 64/2=32 MHz output as PCI clocks.

As a result, Figure 2 illustrates the Cypress Clock software printout using the above configuration.

```
 _____  _____ ___  ___  ___  ___
/ __\ \ / / _ \ _ \ __/ __/ __|
| (__ \ ^ /|  _/   / _|\__ \__ \
 \___| |_| |_| |_|_\___|___/___/ TIMING TECHNOLOGY
================================================
Modification Date: Jun/19/2001
Comments: Sample Design 2 with Network Clock Output
Customer: ZF Micro Devices, Inc.
FAE: Kaido Kevvai
P/N: CY2292FSL-1
```




```
Reference Input: 25.00000 MHz
Operating Voltage: 3.3V
CPLL: --
SPLL: Desired = 48 MHz
UPLL: Desired = 14.31818 MHz
```

CPLL FREQUENCIES

S2:S0	Desired	Actual	PPM	Option
000	64.00000	64.00000	0	--
001	Off	--	--	--
010	Off	--	--	--
011	Off	--	--	--
100	Off	--	--	--
101	Off	--	--	--
110	Off	--	--	--
111	Off	--	--	--

OUTPUT CLOCKS

	Desired	Actual	PPM	Option
CPU	CPLL	CPLL	--	--
CLKA	SPLL (48.00000)	48.00000	0	--
CLKB	UPLL (14.31818)	14.31818	0	--
CLKC	CPLL/2	CPLL/2	--	--
CLKD	CPLL/2	CPLL/2	--	--
XBUF	Ref (25.00000)	25.00000	0	--

ACTUAL OUTPUT FREQUENCIES

S2:S0	CPU	CLKA	CLKB	CLKC	CLKD	XBUF
000	64.00000	48.00000	14.31818	32.00000	32.00000	25.00000
001	Off	48.00000	14.31818	Off	Off	25.00000
010	Off	48.00000	14.31818	Off	Off	25.00000
011	Off	48.00000	14.31818	Off	Off	25.00000
100	Off	48.00000	14.31818	Off	Off	25.00000
101	Off	48.00000	14.31818	Off	Off	25.00000
110	Off	48.00000	14.31818	Off	Off	25.00000
111	Off	48.00000	14.31818	Off	Off	25.00000

```
Entry File: Sample2.ent
CHECKSUM: 231
(Generated by CyClocks(tm) 3.65 - Build #: 3.65.003)
```

Figure 2. Cypress Clock Chip 25 MHz Clock Output