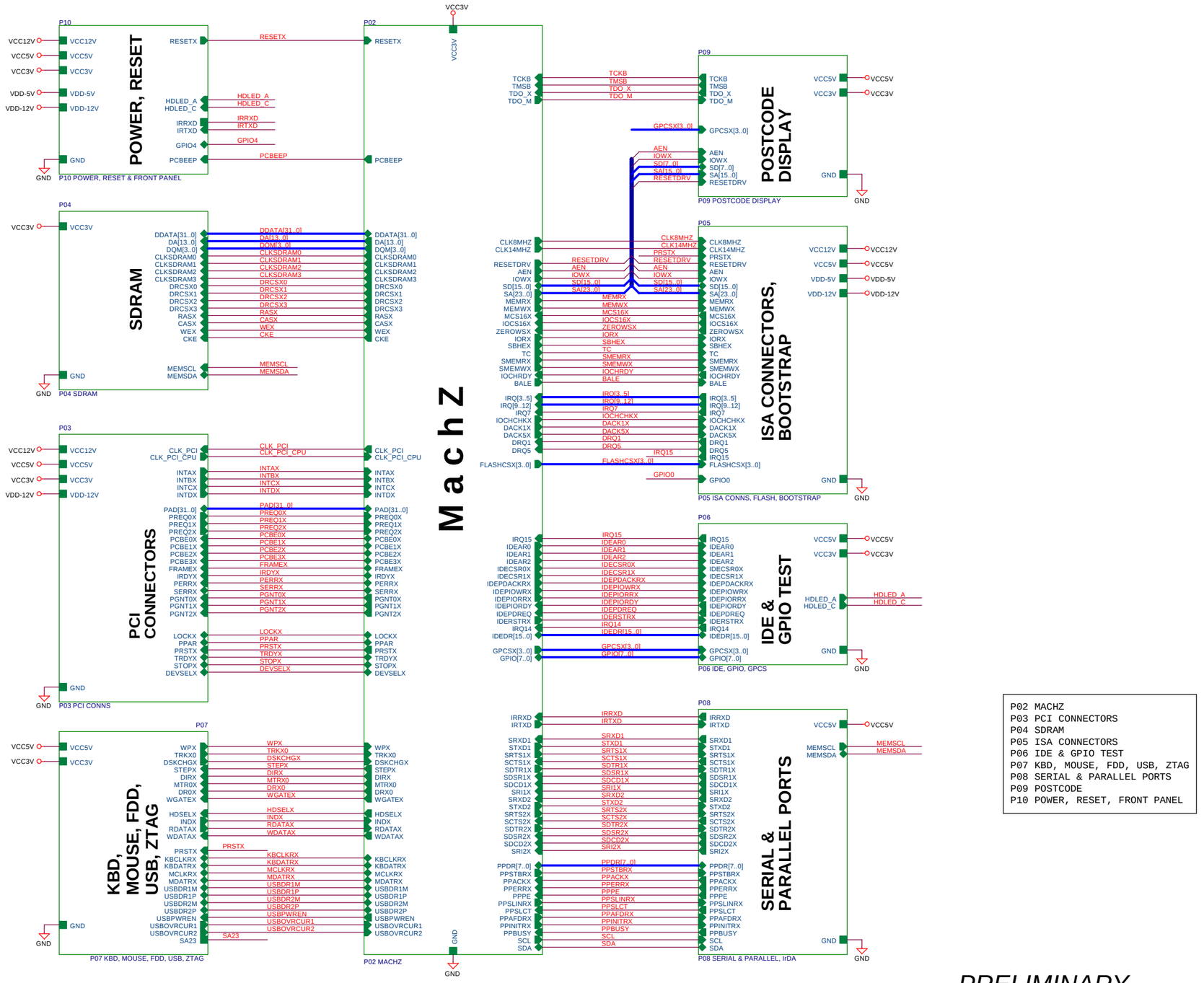
P10
POWER, RESET
P10 POWER, RESET & FRONT PANEL
P04
SDRAM
P04 SDRAM
P03
PCI CONNECTORS
P03 PCI CONNS
P07
KBD, MOUSE, FDD, USB, ZTAG
P07 KBD, MOUSE, FDD, USB, ZTAG
P02
MachZ
P02 MACHZ
P09
POSTCODE DISPLAY
P09 POSTCODE DISPLAY
P05
ISA CONNECTORS, BOOTSTRAP
P05 ISA CONNS, FLASH, BOOTSTRAP
P06
IDE & GPIO TEST
P06 IDE, GPIO, GPCS
P08
SERIAL & PARALLEL PORTS
P08 SERIAL & PARALLEL, IrDA
VCC3V
GND
RESETX
HDLED_A
HDLED_C
IRRXD
IRTXD
GPIO4
PCBEEP
DDATA[31..0]
DA[13..0]
DQM[3..0]
CLKSDRAM0
CLKSDRAM1
CLKSDRAM2
CLKSDRAM3
DRCSX0
DRCSX1
DRCSX2
DRCSX3
RASX
CASX
WEX
CKE
MEMSCL
MEMSDA
CLK_PCI
CLK_PCI_CPU
INTAX
INTBX
INTCX
INTDX
PAD[31..0]
PREQ0X
PREQ1X
PREQ2X
PCBE0X
PCBE1X
PCBE2X
PCBE3X
FRAMEX
IRDYX
PERRX
SERRX
PGNT0X
PGNT1X
PGNT2X
LOCKX
PPAR
PRSTX
TRDYX
STOPX
DEVSELX
WPX
TRKX0
DSKCHGX
STEPX
DIRX
MTR0X
DRX0
WGATEX
HDSELX
INDX
RDATAX
WDATAX
PRSTX
KBCLKRX
KBDATRX
MCLKRX
MDATRX
USBDR1M
USBDR1P
USBDR2M
USBDR2P
USBPWREN
USBOVRCUR1
USBOVRCUR2
SA23
TCKB
TMSB
TDO_X
TDO_M
GPCSX[3..0]
AEN
IOWX
SD[7..0]
SA[15..0]
RESETDRV
CLK8MHZ
CLK14MHZ
PRSTX
SD[15..0]
SA[23..0]
MEMRX
MEMWX
MCS16X
IOCS16X
ZEROWSX
IORX
SBHEX
TC
SMEMRX
SMEMWX
IOCHRDY
BALE
IRQ[3..5]
IRQ[9..12]
IRQ7
IOCHCHKX
DACK1X
DACK5X
DRQ1
DRQ5
IRQ15
FLASHCSX[3..0]
GPIO0
IDEAR0
IDEAR1
IDEAR2
IDECSR0X
IDECSR1X
IDEPDACKRX
IDEPIOWRX
IDEPIORDX
IDEPDREQ
IDERSTRX
IRQ14
IDEDR[15..0]
GPCSX[3..0]
GPIO[7..0]
SRXD1
STXD1
SRTS1X
SCTS1X
SDTR1X
SDSR1X
SDCD1X
SRI1X
SRXD2
STXD2
SRTS2X
SCTS2X
SDTR2X
SDSR2X
SDCD2X
SRI2X
PPDR[7..0]
PPSTBRX
PPACKX
PPERRX
PPPE
PPSLINRX
PPSLCT
PPAFDRX
PPINITRX
PPBUSY
SCL
SDA
VCC12V
VCC5V
VDD-5V
VDD-12V
BD1
8800-0038-03
PCBOARD
P02 MACHZ
P03 PCI CONNECTORS
P04 SDRAM
P05 ISA CONNECTORS, BOOTSTRAP
P06 IDE & GPIO TEST
P07 KBD, MOUSE, USB, ZTAG
P08 SERIAL & PARALLEL PORTS
P09 POSTCODE
P10 POWER, RESET, FRONT PANEL
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(650) 965-3800
APPROVALS
Drawn
K. Kevvai
Checked
Designed by
Artec Design Group
Date
Title
MACHZ EVALUATION 1: MAIN
Rel
01
Size
C
Document nr
9000041303
ZF nr
9400-0038-03-D0
Rev
3
Date:
Friday, January 05, 2001
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of
11

SYS and PCI CLK SPEED

1-3 and 2-4 33MHz (DEFAULT)
3-5 and 4-6 66MHz
1-3 only 80MHz
2-4 only 66MHz

CLK14M SOURCE

1-2 External, BS5 - ON
2-3 GND, BS5 - OFF

RTC 32 kHz INPUT

1-2 Crystal Y2
2-3 GPIO0

SYSCLK SOURCE

1-2 CLK2SYS (REFER TO JP10)
3-4 CLK48MHz
5-6 SELECTABLE

Multiplier Select Table
1 = ON

S0	S1	S2	S3	CLK	MHz
1	1	1	1	TEST	
0	1	1	1	TEST	
1	0	1	1	Input x1	4M
0	0	1	1	Input x3	12M
1	1	0	1	Input x4	16M
0	1	0	1	Input x5	20M
1	0	0	1	Input x6	24M
0	0	0	1	Input x8	32M
1	1	1	0	TEST	
0	1	1	0	pass through	
1	0	1	0	Input x2	8M
0	0	1	0	TEST	
1	1	0	0	Input x8	32M
0	1	0	0	Input x10	40M
1	0	0	0	Input x12	48M
0	0	0	0	Input x16	64M

1-3 and 2-4 MACHZ PCICLKC is input (BS20 = ON)
3-5 and 4-6 MACHZ PCICLKC is output (BS20 = OFF)

PCICLKC SOURCE

KEYBOARD LOCK

1-2 WD OSC EXT
2-3 WD OSC INT

DMA/PCI

1-3 and 2-4 DMA DACK1X/DRQ1 ENABLED
3-5 and 4-6 PCI REQ2X/GNT2X ENABLED

Title	MACHZ
Size	C
Document nr	9000041303
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Rev	3
Date:	Friday, January 05, 2001
Sheet	2 of 11

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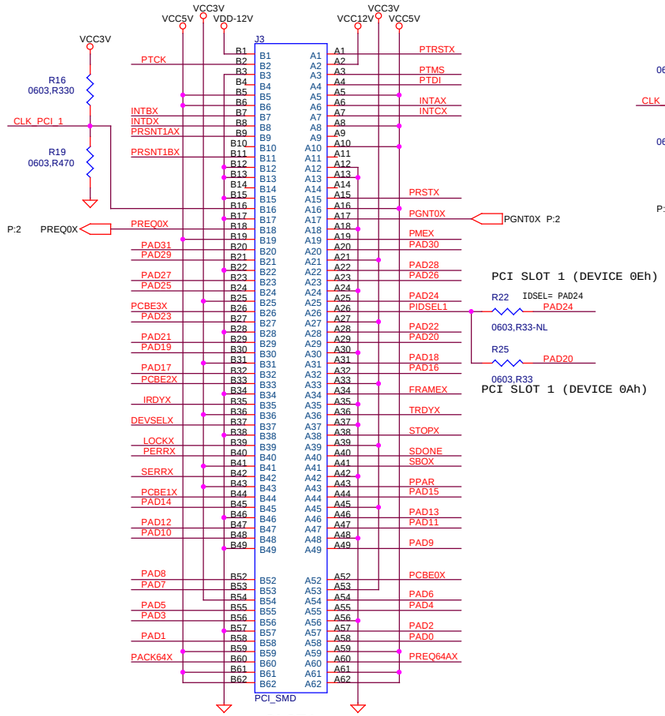

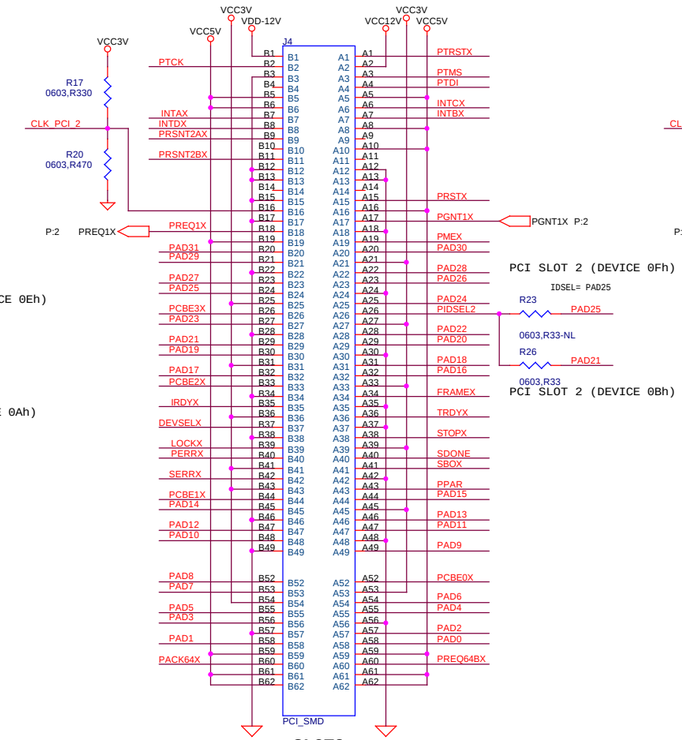

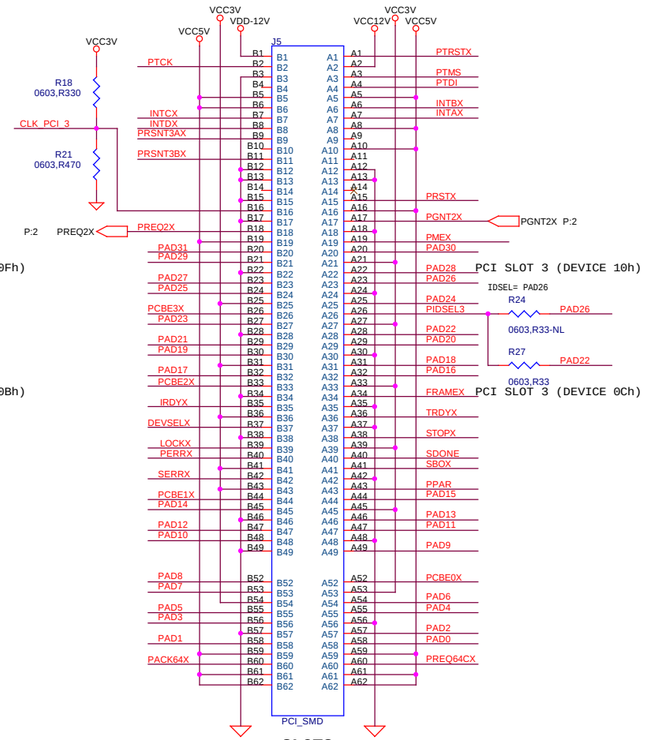

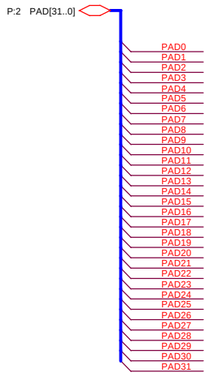

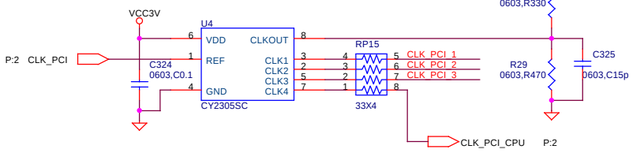

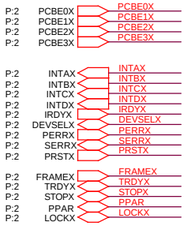

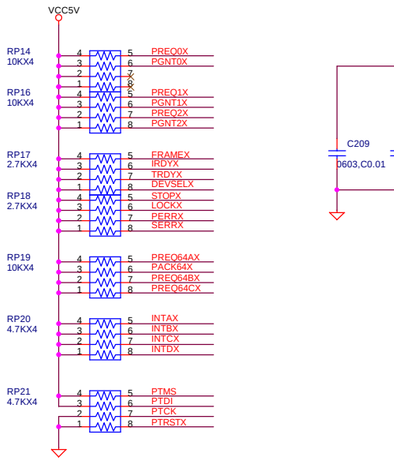

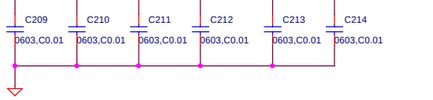

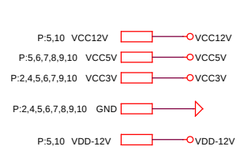

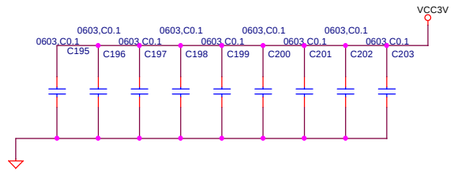

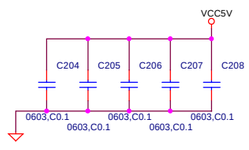

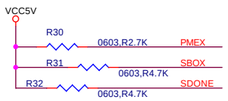

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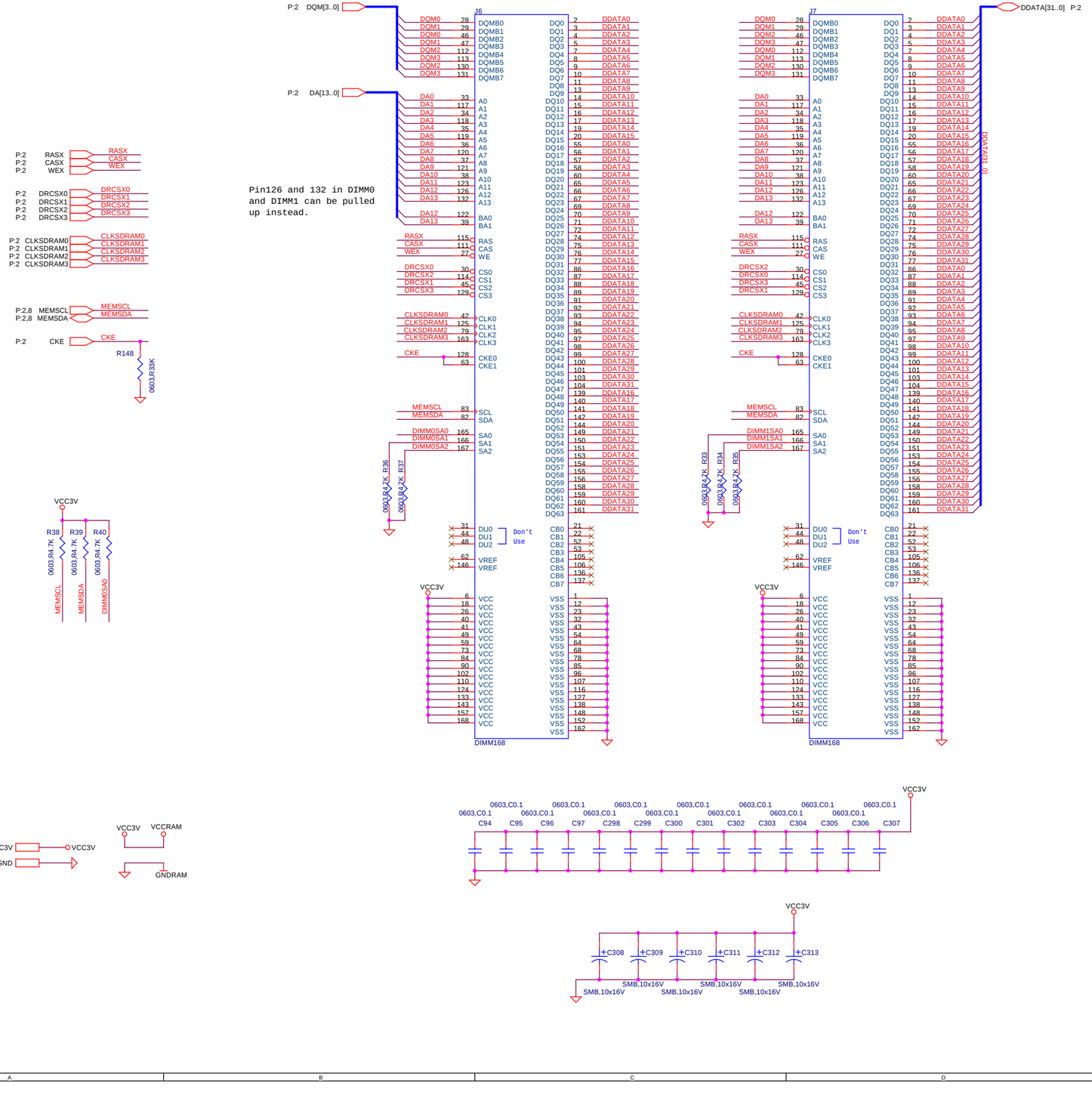
Title	PCI CONNS		
Size C	Document nr 9000041303	ZF nr 9400-0038-03-D0	Rev 3
Date: Friday, January 05, 2001		Sheet 3 of 11	

DIMM0
WITH STANDARD CHIP SELECT ROUTING

DIMM1
WITH ALTERNATIVE CHIP SELECT ROUTING



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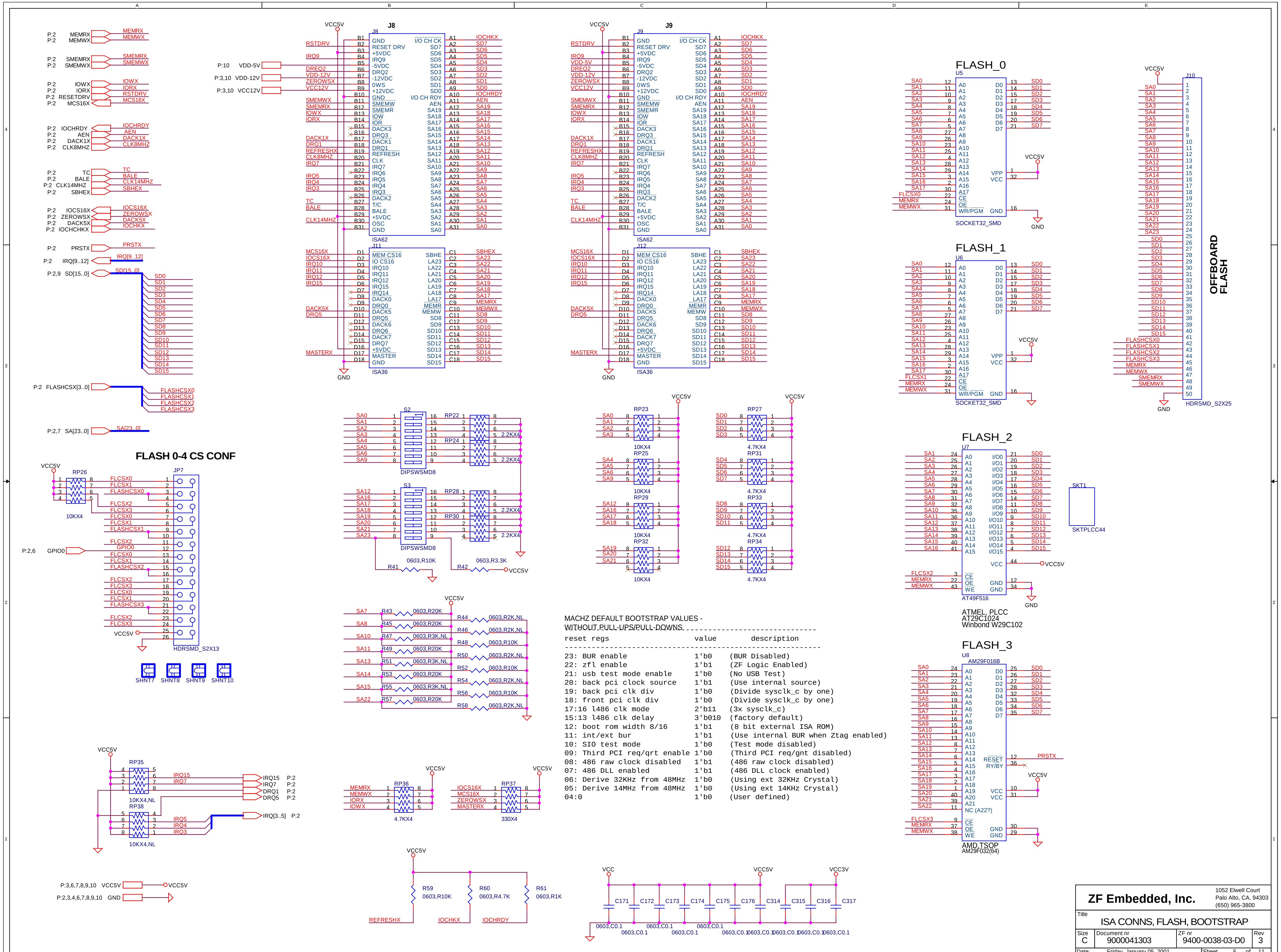
Title	SDRAM
Size C / Document nr 9000041303 / ZF nr 9400-0038-03-D0 / Rev 3	
Date: Friday, January 05, 2001	Sheet 4 of 11



MACHZ DEFAULT BOOTSTRAP VALUES -
WITHOUT PULL-UPS/PULL-DOWNS

reset regs	value	description
23: BUR enable	1'b0	(BUR Disabled)
22: zfl enable	1'b1	(ZF Logic Enabled)
21: usb test mode enable	1'b0	(No USB Test)
20: back pci clock source	1'b1	(Use internal source)
19: back pci clk div	1'b0	(Divide sysclk_c by one)
18: front pci clk div	1'b0	(Divide sysclk_c by one)
17:16 l486 clk mode	2'b11	(3x sysclk_c)
15:13 l486 clk delay	3'b010	(factory default)
12: boot rom width 8/16	1'b1	(8 bit external ISA ROM)
11: int/ext bur	1'b1	(Use internal BUR when Ztag enabled)
10: SIO test mode	1'b0	(Test mode disabled)
09: Third PCI req/qrt enable	1'b0	(Third PCI req/gnt disabled)
08: 486 raw clock disabled	1'b1	(486 raw clock disabled)
07: 486 DLL enabled	1'b1	(486 DLL clock enabled)
06: Derive 32KHz from 48MHz	1'b0	(Using ext 32KHz Crystal)
05: Derive 14MHz from 48MHz	1'b0	(Using ext 14KHz Crystal)
04:0	1'b0	(User defined)

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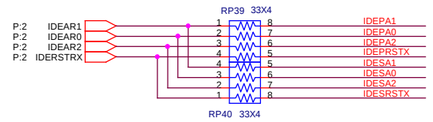
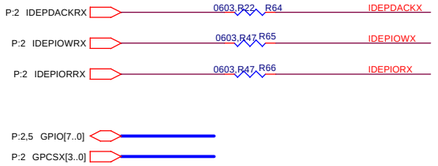
Title: ISA CONNS, FLASH, BOOTSTRAP

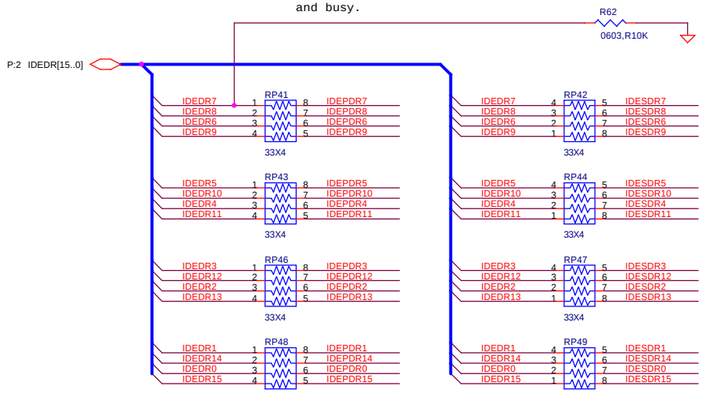
Size	Document nr	ZF nr	Rev
C	9000041303	9400-0038-03-D0	3

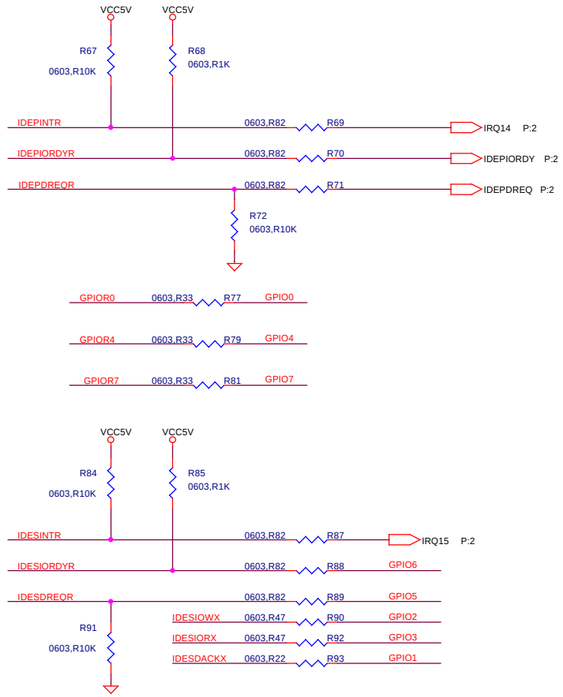
Date: Friday, January 05, 2001

R62 is required per the IDE spec.
IDEDR7 is sampled during drive
detection routines, and if this
signal floats high, detection
software thinks a drive is connected
and busy.

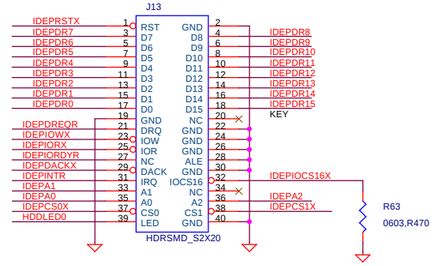




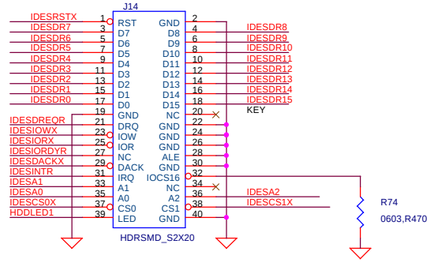


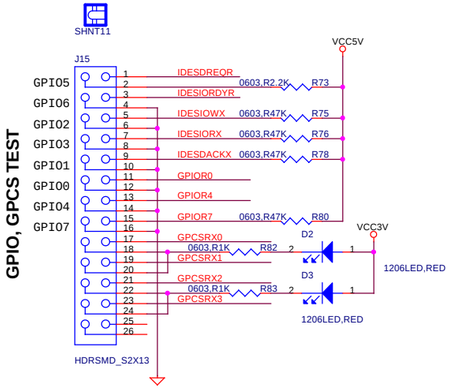


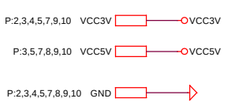
PRIMARY IDE

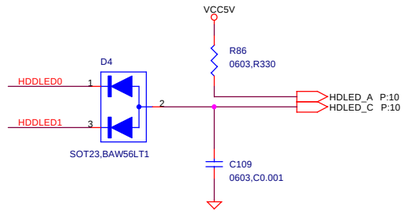


SECONDARY IDE









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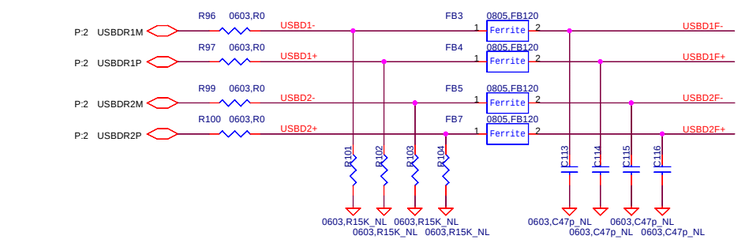
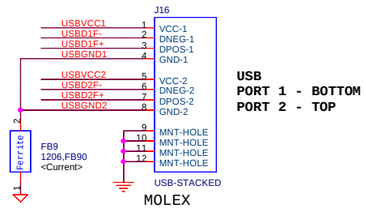
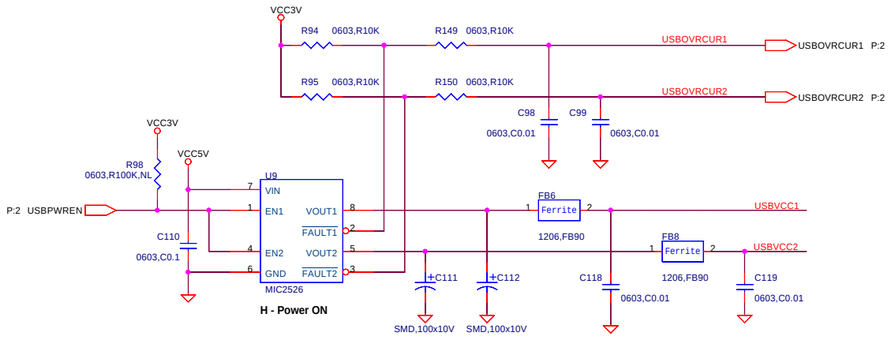
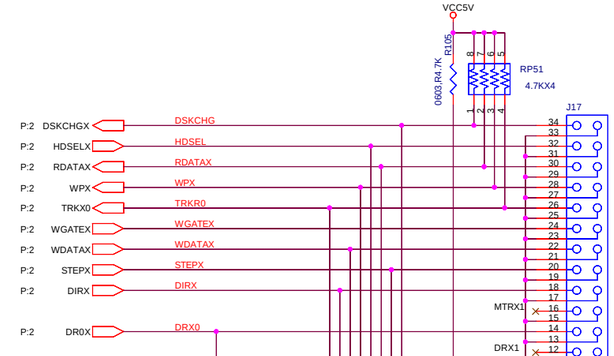
Title: IDE, GPIO, GPCS			
Size: C	Document nr: 9000041303	ZF nr: 9400-0038-03-D0	Rev: 3
Date: Friday, January 05, 2001		Sheet 6 of 11	



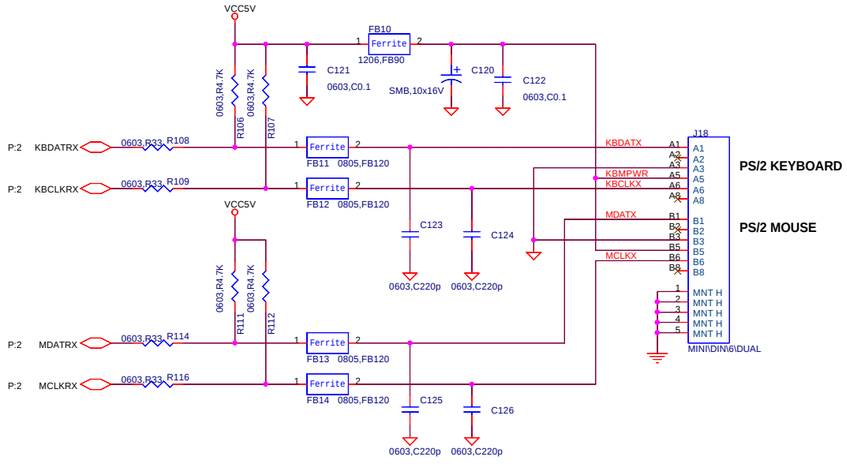


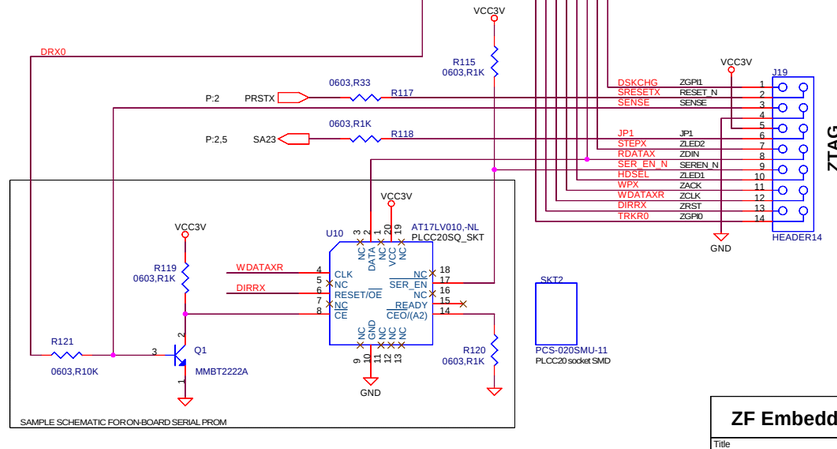
USB
PORT 1 - BOTTOM
PORT 2 - TOP





FLOPPY_DISK





ZTAG

1<ZGPI1
2<RESET_N
3<SENSE
4-GND
5-VCC
6<JP1/SA23
7>ZLED2
8<ZDIN
9<SEREN_N
10>ZLED_1
11<ZACK
12>ZCLCK
13>ZRST
14<ZGPI0

P:2,3,4,5,6,9,10 VCC3V — VCC3V
P:3,5,6,8,9,10 VCC5V — VCC5V
P:2,3,4,5,6,8,9,10 GND

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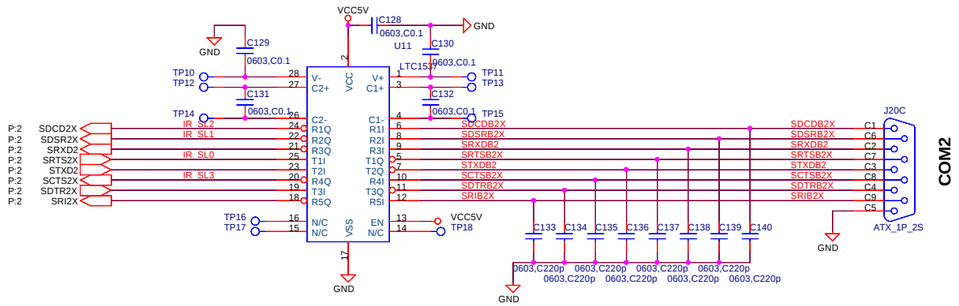
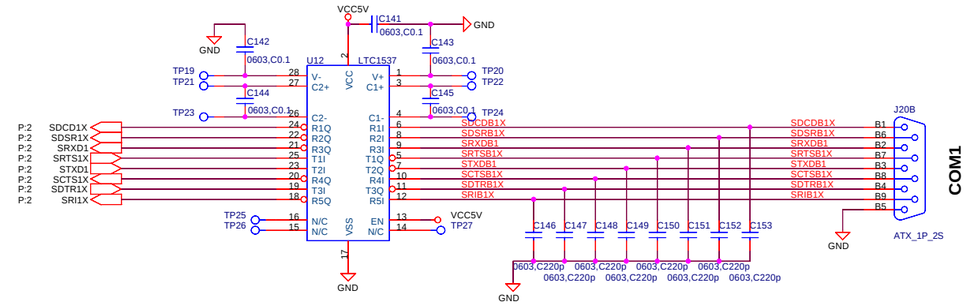
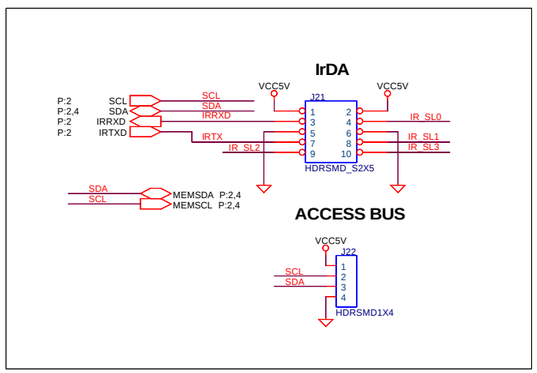
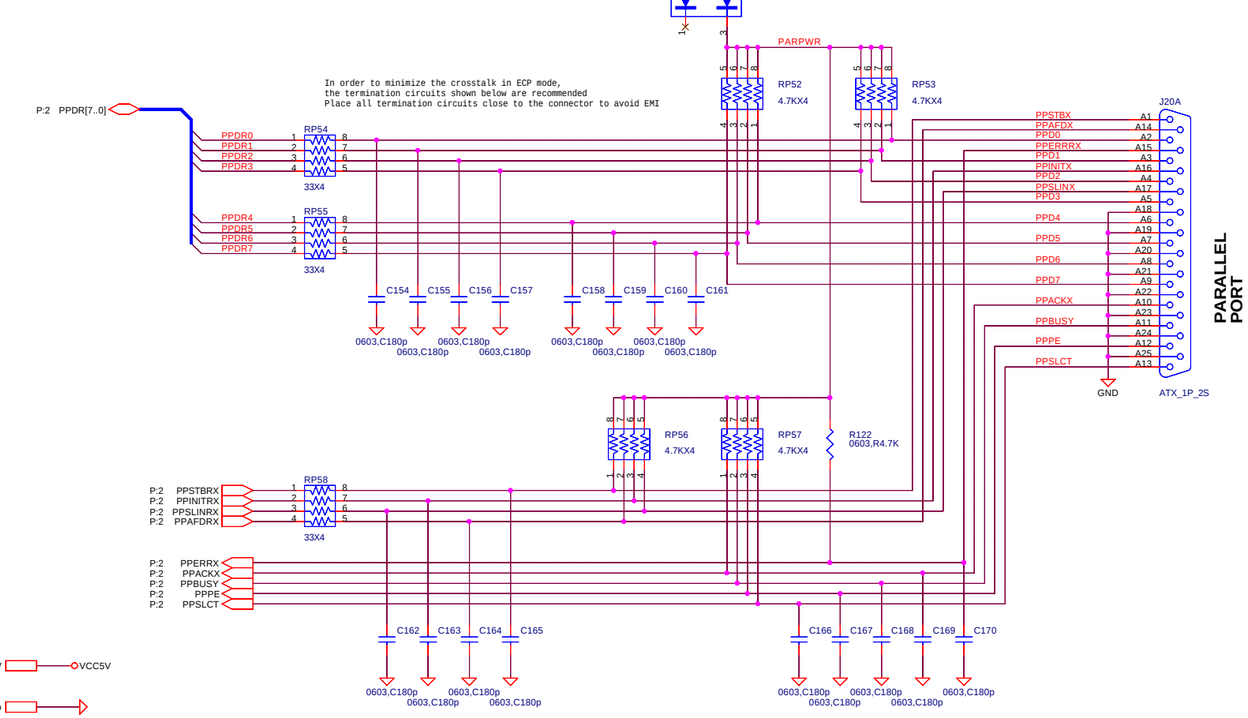
Title: KBD, MOUSE, FDD, USB, ZTAG			
Size: C	Document nr: 9000041303	ZF nr: 9400-0038-03-D0	Rev: 3
Date: Friday, January 05, 2001		Sheet 7 of 11	

RS-232 Tranceivers









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Title	SERIAL & PARALLEL, IrDA, AB		
Size C	Document nr 9000041303	ZF nr 9400-0038-03-D0	Rev 3
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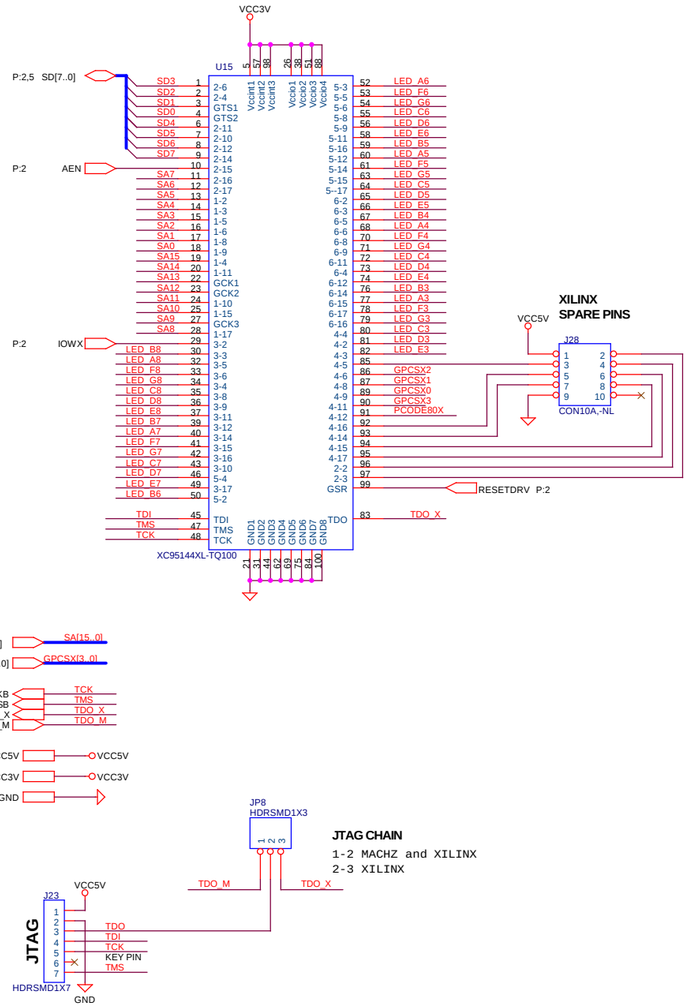
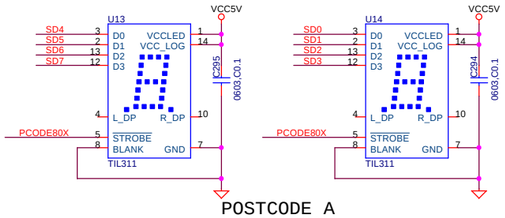
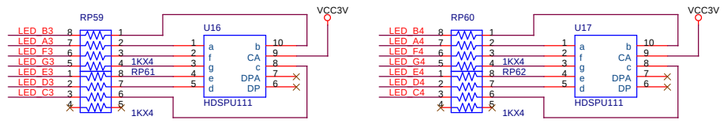
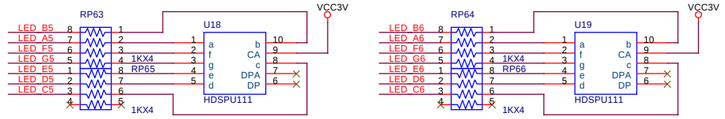




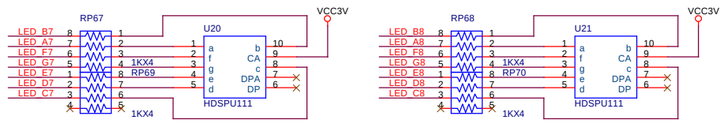
POSTCODE A
(PORT 80)



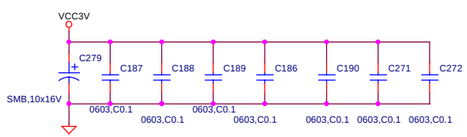
POSTCODE B
(PORT 81)



POSTCODE C
(PORT 82)



POSTCODE D
(PORT 83)



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Title: POSTCODE DISPLAY			
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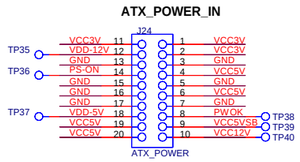
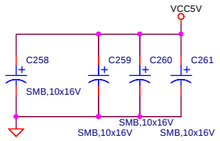
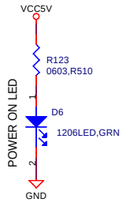
ATX_POWER_IN

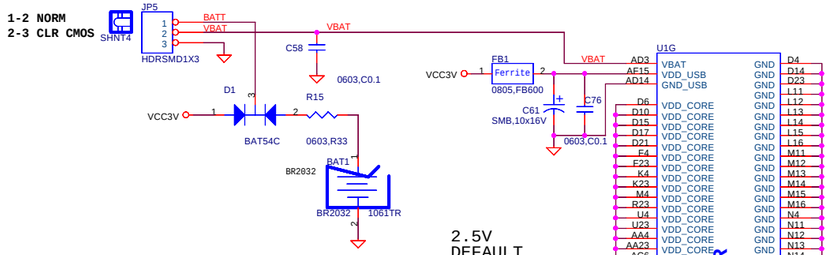


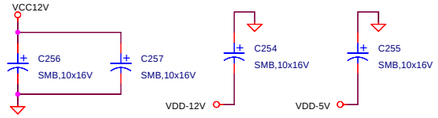


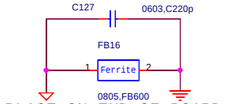


CMOS BATTERY

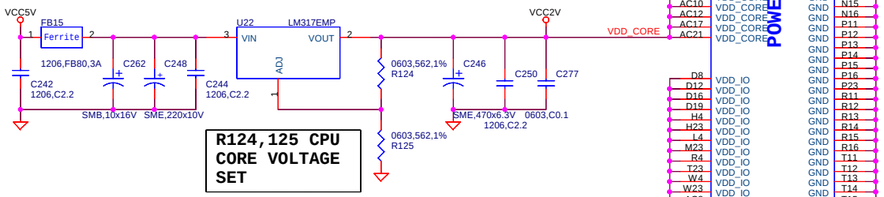
1-2 NORM
2-3 CLR CMOS





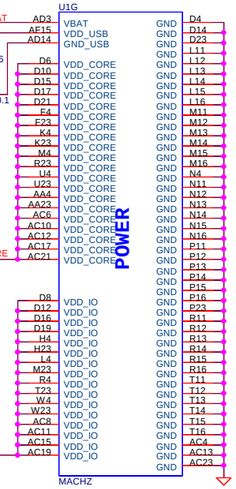


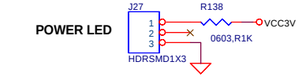
PLACE ON END OF BOARD
CLOSEST TO PSU
CONNECTOR

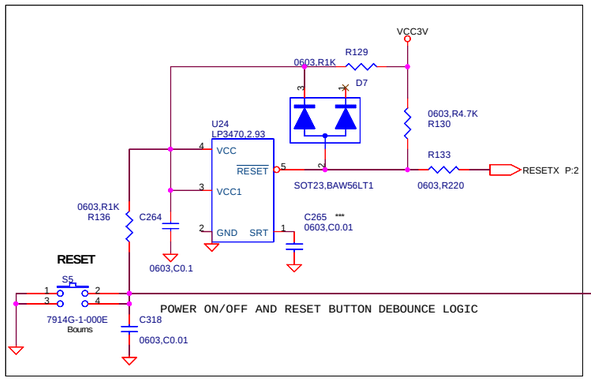


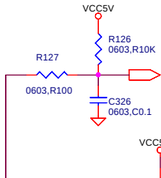
2.5V
DEFAULT

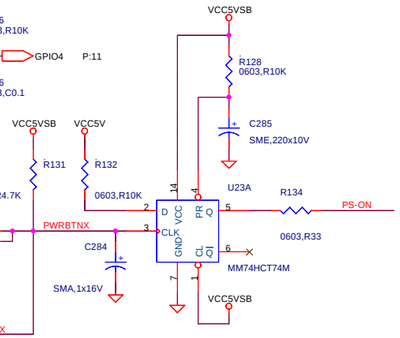
R124,125 CPU CORE VOLTAGE SET

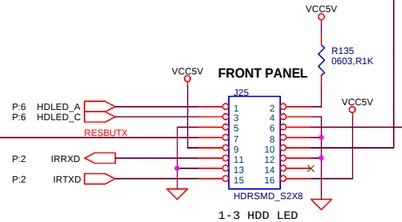




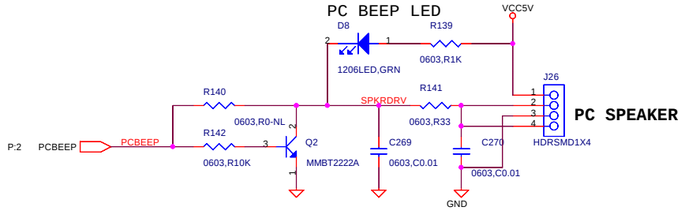


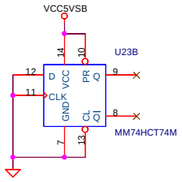


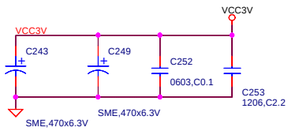


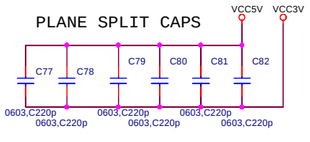


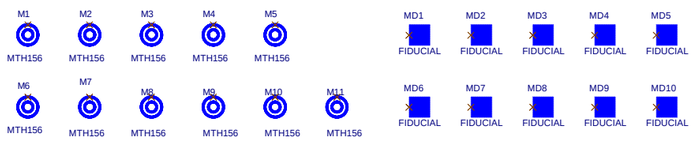
1-3 HDD LED
5-7 RESET BUTTON
9-11-13-15 INFRARED
  9 - VCC
  11 - IR_RXD
  13 - IR_TXD
  15 - GND
2-4 POWER LED (ALSO J27)
6-8 POWER BUTTON
10-12 GPIO4

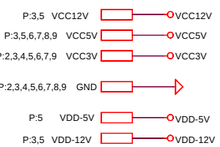


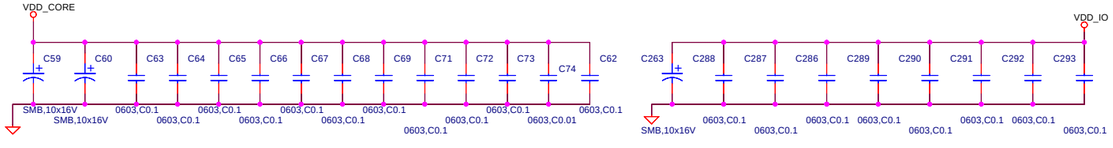


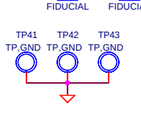












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DEFAULT SETTINGS

(USING EXTERNAL CLOCKS, BIOS IN SOCKET FLASH_0 (U5), 33MHz SYSCLK AND PCICLK, 66MHz CPUCLK)

DEFAULT JUMPER SETTINGS

JP1 CLK14M SOURCE
1-2 External

JP2 WATCHDOG
1-2 External Source

JP3 SYSCLK SOURCE
1-2 CLK2SYS (REFER TO JP10)

JP4 PCICLK SOURCE
1-3 & 2-4 External

JP5 CMOS BATTERY
1-2 Battery connected

JP6 DMA/PCI
3-5 and 4-6 PCI REQ2X/GNT2X ENABLED

JP7 FLASH 0-3 CS CONF
1-3 FLASHCSX0 is connected to FLASH_0 (U5)

JP8 JTAG CHAIN
2-3 Chain has XILINX only

JP9 RTC 32 kHz INPUT
1-2 Crystal Y2

JP10 SYS and PCI CLK SPEED
1-3 and 2-4 33MHz

BOOTSTRAP DIP SWITCHES

04:0	X	(User defined)
05: Derive 14MHz from 48MHz	ON	(Using ext 14KHz)
06: Derive 32KHz from 48MHz	ON	(Using ext 32KHz)
09: Third PCI req/qrt enable	OFF	(Third PCI req/gnt Enabled)
12: boot rom width 8/16	OFF	(8 bit external ISA ROM)
16:17 l486 clk mode	OFF:ON	(2x sysclk_c)
18: front pci clk div	ON	(Divide sysclk_c by one)
19: back pci clk div	ON	(Divide sysclk_c by one)
20: back pci clock source	ON	(Use external source)
21: usb test mode enable	ON	(No USB Test)
23: BUR enable	OFF	(BUR Disabled)

ON-BOARD BOOTSTRAPS

07: 486 DLL enabled	UP	(486 DLL clock enabled)
08: 486 raw clock disabled	UP	(486 raw clock disabled)
10: SIO test mode	DOWN	(Test mode disabled)
11: int/ext bur	UP	(Use internal BUR when Ztag enabled)
13:15 l486 clk delay	TBD	(factory default)
22: zfl enable	UP	(ZF Logic Enabled)

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Palo Alto, CA, 94303
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