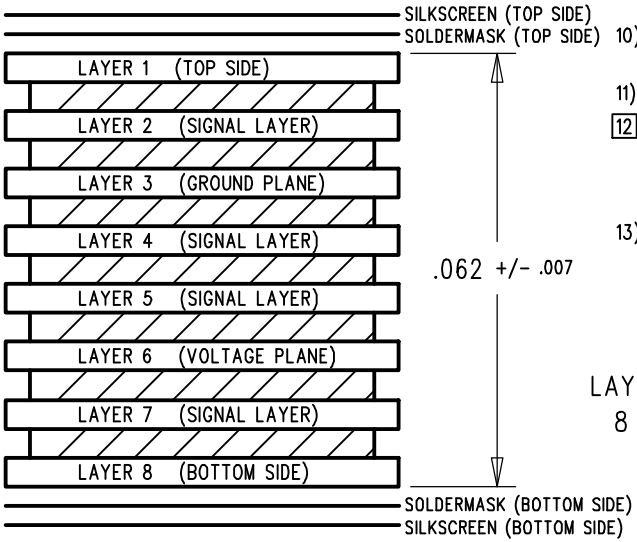


FABRICATION (L24)

| SIZE | QTY | SYM | PLTD |
|------|------|-----|-------|
| 24 | 24 | B | PLTD |
| 79 | 1 | C | PLTD |
| 87 | 1 | D | PLTD |
| 97 | 6 | E | PLTD |
| 40 | 12 | F | PLTD |
| 99 | 4 | G | NPLTD |
| 37 | 17 | H | NPLTD |
| 105 | 2 | I | PLTD |
| 43 | 2 | J | NPLTD |
| 95 | 2 | K | NPLTD |
| 80 | 1 | L | NPLTD |
| 13 | 2408 | M | PLTD |
| 121 | 4 | N | PLTD |
| 45 | 50 | O | PLTD |
| 86 | 2 | P | NPLTD |
| 60 | 10 | Q | PLTD |
| 156 | 6 | R | PLTD |
| 150 | 10 | S | NPLTD |
| 63 | 4 | T | PLTD |
| 51 | 9 | U | PLTD |
| 91 | 4 | V | PLTD |
| 37 | 188 | W | PLTD |
| 90 | 4 | X | NPLTD |
| 67 | 2 | Y | NPLTD |
| 128 | 4 | Z | NPLTD |



LAYER DETAIL
8 LAYERS

NOTES : (UNLESS SPECIFIED OTHERWISE.)

- 1) ALL DIMENSIONS ARE IN INCHES.TOLERANCE IS +/- 0.005 CONFORMING TO IPC-A-600
- 2) HOLE SIZES ARE SPECIFIED IN THOUSANDTHS. HOLE SIZES APPLY AFTER PLATING. HOLE SIZE TOLERANCE TO BE ± 0.003 , UNLESS SPECIFIED OTHERWISE. PLATING TO BE 0.0010 MINIMUM.
- 3) MATERIAL : FR-4-2 NATURAL EPOXY/FIBERGLASS 0.5 OZ. COPPER ALL LAYERS. 2 SIDES PLATED. FINISHED THICKNESS : 0.062 ± 0.006
 $- 0.006$
- 4) APPLY SOLDERMASK OVER BARE COPPER, BOTH SIDES. FINISH ALL EXPOSED COPPER SURFACES WITH 60/40% TIN/LEAD SOLDER, 100u" TO 1000u".
- 5) THE LOCATION OF THE MARKING SHOULD BE ON THE SURFACE OF THE PCB, NOT THE EDGE.
- 6) APPLY SOLDERMASK TO COMPONENT SIDE AND SOLDER SIDE, USING
☐ PC401 OR EQUIVALENT.
☒ LIQUID PHOTO IMAGEABLE.
☐ DRY FILM.
COLOR : GREEN.
USE SEPARATE FILM FOR COMPONENT SIDE AND SOLDER SIDE SOLDERMASKS. FABRICATOR SHALL MAKE NECESSARY MODIFICATIONS TO SOLDERMASK PHOTO PLOT FILES FOR OPTIMAL SOLDERMASK COVERAGE BETWEEN FINE PITCH COMPONENT LEADS.
- 7) APPLY LEGEND TO COMPONENT SIDE USING NON-CONDUCTIVE EPOXY INK. COLOR : WHITE. FABRICATOR SHALL MAKE NECESSARY MODIFICATIONS TO LEGEND PHOTO PLOT FILES TO ENSURE NO LEGEND INK COVERS ANY COMPONENT PAD OR VIA PAD.
- 8) PCB SHALL BE CLEAN AND FREE FROM DIRT, OIL, FINGERPRINTS, CORROSION, AND ANY OTHER FOREIGN MATERIAL.
- 9) MODIFIED PHOTO PLOT FILES ARE TO BE RETURNED BEFORE ORDER DELIVERED.
- 10) FABRICATOR HAS APPROVAL TO REMOVE NON-FUNCTIONAL PADS FROM INNER LAYERS.
- 11) BOW AND TWIST SHALL BE LESS THAN 0.005" PER INCH.
- 12) ALL PRINTED CIRCUIT BOARD NETS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS. MARK TEST VERIFICATION STAMP APPROXIMATELY WHERE SHOWN, ALONG EDGE OF PCB, USING WHITE INK.
- 13) FABRICATION OF P.W.B. TO COMPLY WITH IPC-A-600, CLASS II , CURRENT REVISION.

| APPROVALS | | DATE | ZF Linux Devices, Inc. 1052 Elwell Court Palo Alto,CA 94303 (650) 965-3800 | | | |
|-----------|------------------------|----------|--|-------------|--------------|------------|
| DRAWN: | Elli Puusepp | 11/03/00 | | | | |
| CHECKED: | Alar Kuusik | 11/03/00 | INTERNET APPLIANCE 2 FABRICATION | | | RELEASE 01 |
| PROJ MGR: | ARTEC DG | | | | | REVISION 3 |
| CLIENT: | ZF Linux Devices, Inc. | SIZE B | DRAWING NUMBER 9400-0048-03-X3 | SCALE 1 : 1 | SHEET 1 OF 1 | |

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9400-0048-03

DATE : 11/03/2000